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Polycrystalline Silicon Layer With Nano-grain Structure and Method of Manufacture

Abstract

A method of forming polycrystalline silicon with ultra-small grain sizes employs a differential heating of the upper and lower sides of the substrate of a CVD apparatus, in which the lower side of the substrate receives considerably more power than the upper side, preferable more than 75% of the power; and in which the substrate is maintained during deposition at a temperature more than 50 °C above the 550°C crystallization temperature of silicon.